To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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April 1st, 2010
Renesas Electronics Corporation

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MOS INTEGRATED CIRCUIT
μPD78F0988

8-BIT SINGLE-CHIP MICROCONTROLLER

The μPD78F0988 is a member of the μPD780988 Subseries of the 78K/0 Series that substitute flash memory for the internal ROM of the μPD780988. Flash memory can be written or erased electrically without having to remove it from board. Therefore, the μPD78F0988 is best suited for evaluation in system development, small-scale production, or systems likely to be upgraded frequently.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μ**PD780988 Subseries User's Manual:** U13029E
78K/0 Series Instructions User's Manual: U12326E

FEATURES
- Pin-compatible with mask ROM version (except V_{PP} pin)
- Flash memory: 60 Kbytes**Note 1**
- Internal high-speed RAM: 1024 bytes
- Internal expansion RAM: 1024 bytes**Note 2**
- Operable in the same supply voltage range as the mask ROM version (V_{DD} = 4.0 to 5.5 V)

Notes 1. The capacity of the flash memory can be changed with the internal memory size switching register (IMS).
   2. The capacity of the internal expansion RAM can be changed with the internal expansion RAM size switching register (IXS).

Remark For the differences between the flash memory versions and the mask ROM versions, refer to
   1. DIFFERENCES BETWEEN μPD78F0988 AND MASK ROM VERSIONS.

ORDERING INFORMATION

Part Number	Package
μPD78F0988CW	64-pin plastic shrink DIP (750 mil)
μPD78F0988GC-AB8	64-pin plastic QFP (14 $\times$ 14 mm)

The mark ★ shows major revised points.

★ 78K/0 SERIES LINEUP

The products in the 78K/0 Series are listed below. The names enclosed in boxes are subseries names.

	In mass-production
	Under development

Y subseries products are compatible with I²C bus.

78K/0 Series

For control

100-pin	μPD78075B		μPD78078 with reduced EMI noise
100-pin	μPD78078	μPD78078Y	μPD78054 with timer and enhanced external interface function
100-pin	μPD78070A	μPD78070AY	ROM-less version of the μPD78078
100-pin		μPD780018AY	μPD78078Y with enhanced serial I/O and restricted function
80-pin	μPD780058	μPD780058Y	μPD78054 with enhanced serial I/O
80-pin	μPD78058F	μPD78058FY	μPD78054 with reduced EMI noise
80-pin	μPD78054	μPD78054Y	μPD78018F with UART and D/A converter, and enhanced I/O
80-pin	μPD780065		μPD780024A with expanded RAM
64-pin	μPD780078	μPD780078Y	μPD780034A with timer and enhanced serial I/O
64-pin	μPD780034A	μPD780034AY	μPD780024A with enhanced A/D converter
64-pin	μPD780024A	μPD780024AY	μPD78018F with enhanced serial I/O
64-pin	μPD78014H		μPD78018F with reduced EMI noise
64-pin	μPD78018F	μPD78018FY	Basic subseries for control
42/44-pin	μPD78083		On-chip UART and capable of low-voltage (1.8 V) operation

For inverter control

64-pin	μPD780988	On-chip inverter control circuit and UART, EMI noise reduced product

For FIP™ driving

100-pin	μPD780208	μPD78044F with enhanced I/O and FIP C/D, Total display output: 53
100-pin	μPD780228	μPD78044H with enhanced I/O and FIP C/D, Total display output: 48
80-pin	μPD780232	For panel control and on-chip FIP C/D, Total display output: 53
80-pin	μPD78044H	μPD78044F with N-ch open-drain I/O, Total display output: 34
80-pin	μPD78044F	Basic subseries for FIP driving, Total display output: 34

For LCD driving

100-pin	μPD780308	μPD780308Y	μPD78064 with enhanced SIO and expanded ROM and RAM
100-pin	μPD78064B		μPD78064 with reduced EMI noise
100-pin	μPD78064	μPD78064Y	Basic subseries for LCD driving and on-chip UART

Call ID supporting

80-pin	μPD780841	On-chip Call ID function and simple DTMF, EMI noise reduced product

Bus interface supporting

100-pin	μPD780948	On-chip DCAN controller
80-pin	μPD78098B	μPD78054 with IEBus™ controller, EMI noise reduced product
80-pin	μPD780701Y	On-chip DCAN/IEBus controller
80-pin	μPD780833Y	On-chip J1850 (CLASS2) controller
64-pin	μPD780814	Specialized in DCAN controller

For meter control

100-pin	μPD780958	For industrial meter control
80-pin	μPD780973	On-chip controller/driver for automobile meter driving
80-pin	μPD780824	For automobile meter driving and on-chip DCAN controller
80-pin	μPD780955	Ultra low power consumption and on-chip UART

The major functional differences among the subseries are listed below.

Function / Subseries Name		ROM Capacity	Timer				8-bit A/D	10-bit A/D	8-bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-bit	16-bit	Watch	WDT							
For control	μPD78075B	32 K to 40 K	4 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	3 ch (UART: 1 ch)	88	1.8 V	√
	μPD78078	48 K to 60 K											
	μPD78070A	–									61	2.7 V	
	μPD780058	24 K to 60 K	2 ch							3 ch (time-division UART: 1 ch)	68	1.8 V	
	μPD78058F	48 K to 60 K								3 ch (UART: 1 ch)	69	2.7 V	
	μPD78054	16 K to 60 K										2.0 V	
	μPD780065	40 K to 48 K							–	4 ch (UART: 1 ch)	60	2.7 V	
	μPD780078	48 K to 60 K		2 ch			–	8 ch		3 ch (UART: 2 ch)	52	1.8 V	
	μPD780034A	8 K to 32 K		1 ch						3 ch (UART: 1 ch)	51		
	μPD780024A						8 ch	–					
	μPD78014H									2 ch	53		
	μPD78018F	8 K to 60 K											
	μPD78083	8 K to 16 K		–	–					1 ch (UART: 1 ch)	33		–
For inverter control	μPD780988	16 K to 60 K	3 ch	**Note**	–	1 ch	–	8 ch	–	3 ch (UART: 2 ch)	47	4.0 V	√
For FIP driving	μPD780208	32 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	–	–	2 ch	74	2.7 V	–
	μPD780228	48 K to 60 K	3 ch	–	–					1 ch	72	4.5 V	
	μPD780232	16 K to 24 K					4 ch			2 ch	40		
	μPD78044H	32 K to 48 K	2 ch	1 ch	1 ch		8 ch			1 ch	68	2.7 V	
	μPD78044F	16 K to 40 K								2 ch			
For LCD driving	μPD780308	48 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	–	–	3 ch (time-division UART: 1 ch)	57	2.0 V	–
	μPD78064B	32 K								2 ch (UART: 1 ch)			
	μPD78064	16 K to 32 K											
Call ID supporting	μPD780841	24 K to 32 K	2 ch	–	1 ch	1 ch	2 ch	–	–	2 ch (UART: 1 ch)	61	2.7 V	–
Bus interface supporting	μPD780948	60 K	2 ch	2 ch	1 ch	1 ch	8 ch	–	–	3 ch (UART: 1 ch)	79	4.0 V	√
	μPD78098B	40 K to 60 K		1 ch					2 ch		69	2.7 V	–
	μPD780814	32 K to 60 K		2 ch			12 ch		–	2 ch (UART: 1 ch)	46	4.0 V	
For meter control	μPD780958	48 K to 60 K	4 ch	2 ch	–	1 ch	–	–	–	2 ch (UART: 1 ch)	69	2.2 V	–
	μPD780973	24 K to 32 K	3 ch	1 ch	1 ch		5 ch				56	4.5 V	
	μPD780824	32 K to 60 K									59	4.0 V	
	μPD780955	40 K	6 ch		–		1 ch			2 ch (UART: 2 ch)	50	2.2 V	

Note 16-bit timer: 2 channels
10-bit timer: 1 channel

OVERVIEW OF FUNCTIONS

	Item	Function
Internal memory	Flash memory	60 Kbytes[Note 1]
	High-speed RAM	1024 bytes
	Expansion RAM	1024 bytes[Note 2]
Memory space		64 Kbytes
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Instruction cycle		On-chip instruction execution time variable function
		0.24 μs/0.48 μs/0.96 μs/1.9 μs/3.8 μs (@ 8.38-MHz operation with system clock)
Instruction set		• 16-bit operation
		• Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits)
		• Bit manipulation (set, reset, test, Boolean operation)
		• BCD adjust, etc.
I/O ports		Total: 47
		• CMOS inputs: 8
		• CMOS I/Os: 39
Real-time output ports		• 8 bits × 1 or 4 bits × 2
		• 6 bits × 1 or 4 bits × 1
A/D converter		• 10-bit resolution × 8 channels
		• Power supply voltage: AV_{DD} = 4.0 to 5.5 V
Serial interface		• UART mode: 2 channels
		• 3-wire serial I/O mode: 1 channel
Timer		• 16 bit timer/event counter: 2 channels
		• 8-bit timer/event counter: 3 channels
		• 10-bit inverter control timer: 1 channel
		• Watchdog timer: 1 channel
★ Timer output		11 (general-purpose outputs: 5 and inverter control outputs: 6)
Vectored interrupt sources	Maskable	Internal: 16, external: 8
	Non-maskable	Internal: 1
	Software	1
Power supply voltage		V_{DD} = 4.0 to 5.5 V
Operating ambient temperature		T_A = −40 to +85°C
Package		• 64-pin plastic shrink DIP (750 mil)
		• 64-pin plastic QFP (14 × 14 mm)

Notes 1. The capacity of the flash memory can be changed with the internal memory size switching register (IMS).

2. The capacity of the internal expansion RAM can be changed with the internal expansion RAM size switching register (IXS).

PIN CONFIGURATION (Top View)

- **64-Pin Plastic Shrink DIP (750 mil)**
  μPD78F0988CW
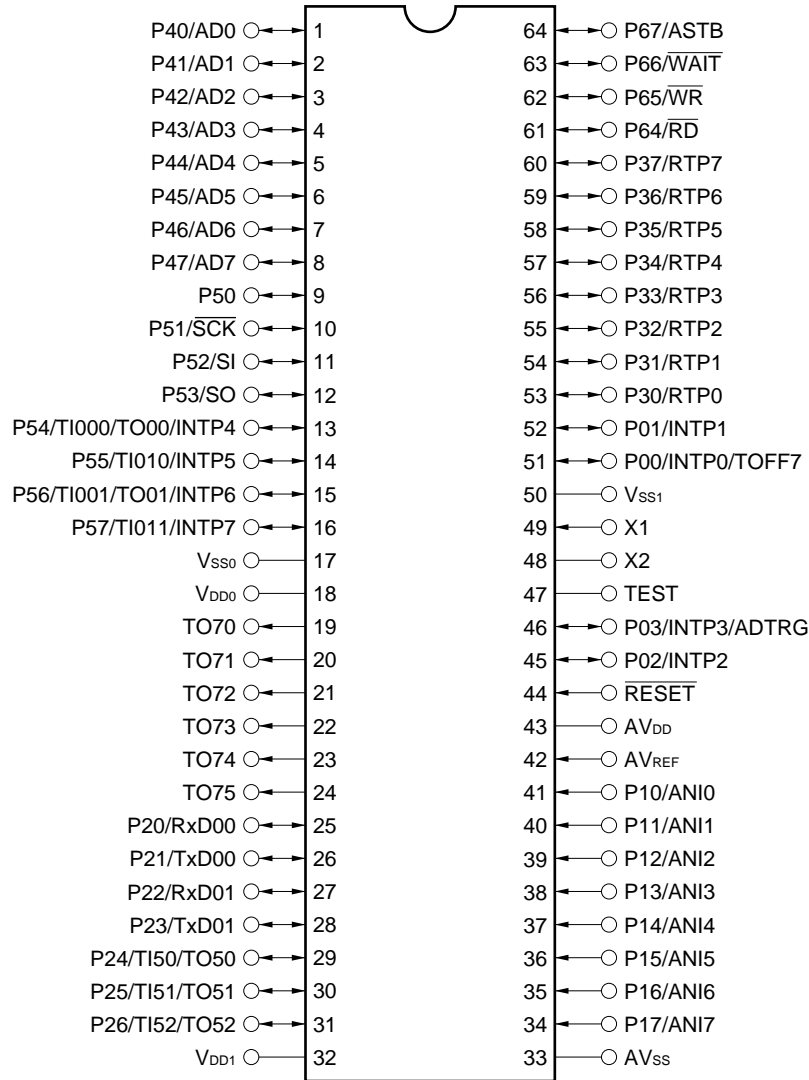
Pin			Pin
P40/AD0	1	64	P67/ASTB
P41/AD1	2	63	P66/$\overline{\text{WAIT}}$
P42/AD2	3	62	P65/$\overline{\text{WR}}$
P43/AD3	4	61	P64/$\overline{\text{RD}}$
P44/AD4	5	60	P37/RTP7
P45/AD5	6	59	P36/RTP6
P46/AD6	7	58	P35/RTP5
P47/AD7	8	57	P34/RTP4
P50	9	56	P33/RTP3
P51/$\overline{\text{SCK}}$	10	55	P32/RTP2
P52/SI	11	54	P31/RTP1
P53/SO	12	53	P30/RTP0
P54/TI000/TO00/INTP4	13	52	P01/INTP1
P55/TI010/INTP5	14	51	P00/INTP0/TOFF7
P56/TI001/TO01/INTP6	15	50	V_{SS1}
P57/TI011/INTP7	16	49	X1
V_{SS0}	17	48	X2
V_{DD0}	18	47	TEST
TO70	19	46	P03/INTP3/ADTRG
TO71	20	45	P02/INTP2
TO72	21	44	$\overline{\text{RESET}}$
TO73	22	43	AV_{DD}
TO74	23	42	AV_{REF}
TO75	24	41	P10/ANI0
P20/RxD00	25	40	P11/ANI1
P21/TxD00	26	39	P12/ANI2
P22/RxD01	27	38	P13/ANI3
P23/TxD01	28	37	P14/ANI4
P24/TI50/TO50	29	36	P15/ANI5
P25/TI51/TO51	30	35	P16/ANI6
P26/TI52/TO52	31	34	P17/ANI7
V_{DD1}	32	33	AV_{SS}

★ **Caution** **In the normal operation mode, connect the V_{PP} pin directly to V_{SS0}.**

Remark When the μPD78F0988 is used in applications where the noise generated inside the microcontroller needs to be reduced, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

- **64-Pin Plastic QFP (14 × 14 mm)**
  *µ*PD78F0988GC-AB8

Top pins (64–49): P47/AD7, P46/AD6, P45/AD5, P44/AD4, P43/AD3, P42/AD2, P41/AD1, P40/AD0, P67/ASTB, P66/WAIT, P65/WR, P64/RD, P37/RTP7, P36/RTP6, P35/RTP5, P34/RTP4

Left pins (1–16): P50, P51/SCK, P52/SI, P53/SO, P54/TI000/TO00/INTP4, P55/TI010/INTP5, P56/TI001/TO01/INTP6, P57/TI011/INTP7, Vss0, Vdd0, TO70, TO71, TO72, TO73, TO74, TO75

Right pins (48–33): P33/RTP3, P32/RTP2, P31/RTP1, P30/RTP0, P01/INTP1, P00/INTP0/TOFF7, Vss1, X1, X2, TEST, P03/INTP3/ADTRG, P02/INTP2, RESET, AVdd, AVref, P10/ANI0

Bottom pins (17–32): P20/RxD00, P21/TxD00, P22/RxD01, P23/TxD01, P24/TI50/TO50, P25/TI51/TO51, P26/TI52/TO52, Vdd1, AVss, P17/ANI7, P16/ANI6, P15/ANI5, P14/ANI4, P13/ANI3, P12/ANI2, P11/ANI1
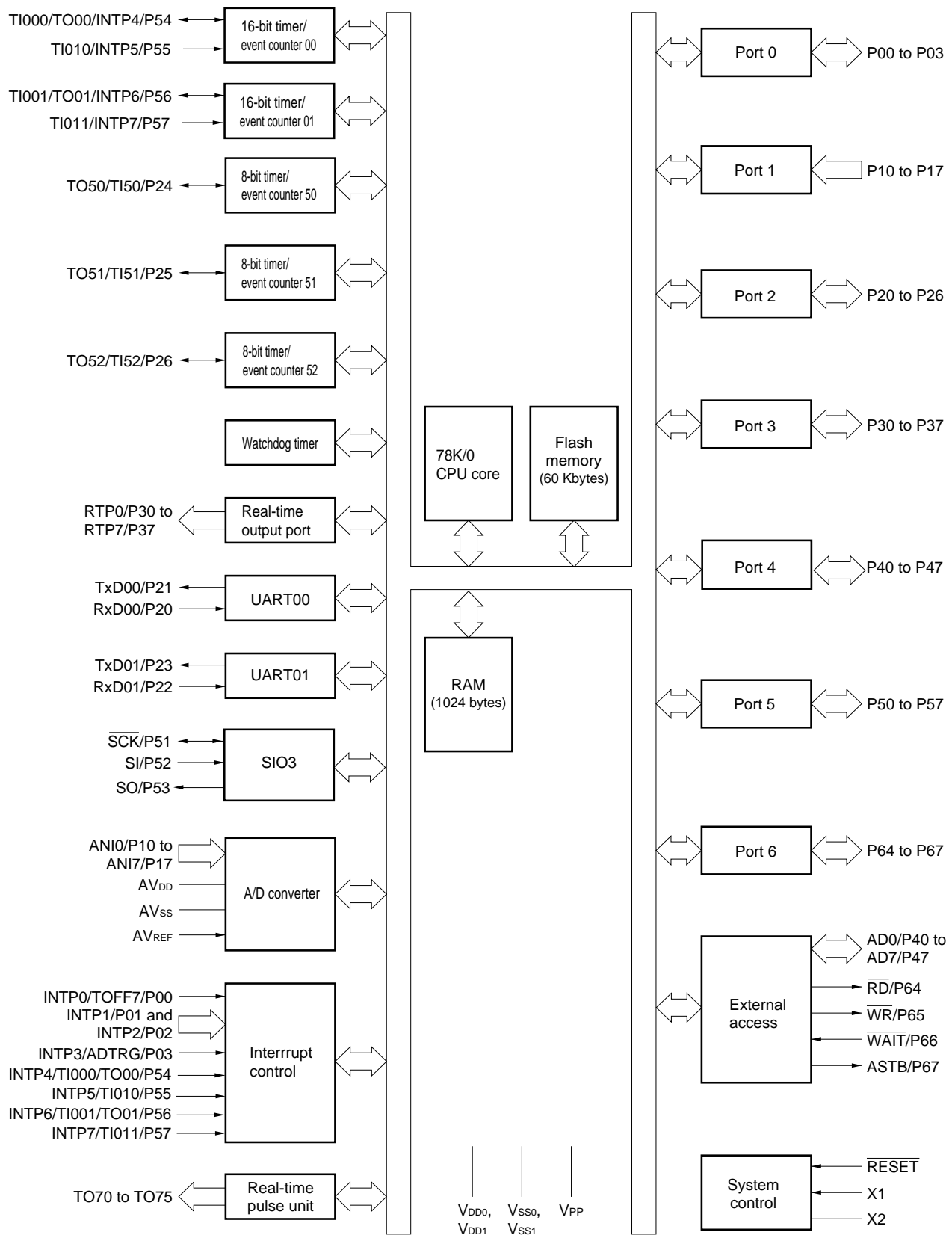
★ **Caution** In the normal operation mode, connect the Vpp pin directly to Vss0.

Remark When the *µ*PD78F0988 is used in applications where the noise generated inside the microcontroller needs to be reduced, the implementation of noise reduction measures, such as supplying voltage to Vdd0 and Vdd1 individually and connecting Vss0 and Vss1 to different ground lines, is recommended.

AD0 to AD7:	Address/Data Bus		RxD00, RxD01:	Receive Data
ADTRG:	AD Trigger Input		$\overline{\text{SCK}}$:	Serial Clock
ANI0 to ANI7:	Analog Input		SI:	Serial Input
ASTB:	Address Strobe		SO:	Serial Output
AV_{DD}:	Analog Power Supply		TI000, TI001,	
AV_{REF}:	Analog Reference Voltage		TI010, TI011,	
AV_{SS}:	Analog Ground		TI50 to TI52:	Timer Input
INTP0 to INTP7:	External Interrupt Input		TO00, TO01,	
P00 to P03:	Port 0		TO50 to TO52,	
P10 to P17:	Port 1		TO70 to TO75:	Timer Output
P20 to P26:	Port 2		TOFF7:	Timer Output Off
P30 to P37:	Port 3		TxD00, TxD01:	Transmit Data
P40 to P47:	Port 4		V_{DD0}, V_{DD1}:	Power Supply
P50 to P57:	Port 5		V_{PP}:	Programming Power Supply
P64 to P67:	Port 6		V_{SS0}, V_{SS1}:	Ground
$\overline{\text{RD}}$:	Read Strobe		$\overline{\text{WAIT}}$:	Wait
$\overline{\text{RESET}}$:	Reset		$\overline{\text{WR}}$:	Write Strobe
RTP0 to RTP7:	Real-time Port		X1, X2:	Crystal

BLOCK DIAGRAM

CONTENTS

1. DIFFERENCES BETWEEN μPD78F0988 AND MASK ROM VERSIONS

The μPD78F0988 is a product with a flash memory which enables on-board writing, erasing and rewriting of programs.

Except for flash memory specifications, the same functions as those of mask ROM versions can be obtained by setting the internal memory size switching register (IMS) and internal expansion RAM size switching register (IXS).

Table 1-1 shows the differences between the flash memory version (μPD78F0988) and mask ROM versions
★ (μPD780982, 780983, 780984, 780986, 780988).

★ **Table 1-1.   Differences between μPD78F0988 and Mask ROM Versions**

Item	μPD78F0988	Mask ROM Versions
Internal ROM structure	Flash memory	Mask ROM
Internal ROM capacities	60 Kbytes	μPD780982: 16 Kbytes μPD780983: 24 Kbytes μPD780984: 32 Kbytes μPD780986: 48 Kbytes μPD780988: 60 Kbytes
Internal expansion RAM capacities	1024 bytes	μPD780982: None μPD780983: None μPD780984: None μPD780986: 1024 bytes μPD780988: 1024 bytes
Change of internal ROM capacity with internal memory size switching register (IMS)	Available[Note 1]	Not available
Change of internal expansion RAM capacity with internal expansion RAM size switching register (IXS)	Available[Note 2]	Not available
TEST pin	Not provided	Provided
V_{PP} pin	Provided	Not provided

Notes 1. Flash memory capacity becomes 60 Kbytes by $\overline{\text{RESET}}$ input.

2. Internal expansion RAM capacity becomes 0 byte by $\overline{\text{RESET}}$ input.

Caution   There are differences in noise immunity and noise radiation between the flash memory and mask ROM versions. When pre-producing an application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluations for the commercial samples (not engineering samples) of the mask ROM versions.

2. PIN FUNCTIONS

2.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0	Input	INTP0/TOFF7
P01		4-bit I/O port		INTP1
P02		Input/output can be specified in 1-bit units.		INTP2
P03		An on-chip pull-up resistor can be specified by means of software.		INTP3/ADTRG
P10 to P17	Input	Port 1 8-bit input only port	Input	ANI0 to ANI7
P20	I/O	Port 2	Input	RxD00
P21		7-bit I/O port		TxD00
P22		Input/output can be specified in 1-bit units.		RxD01
P23		An on-chip pull-up resistor can be specified by means of software.		TxD01
P24				TI50/TO50
P25				TI51/TO51
P26				TI52/TO52
P30 to P37	I/O	Port 3 8-bit I/O port Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.	Input	RTP0 to RTP7
P40 to P47	I/O	Port 4 8-bit I/O port Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.	Input	AD0 to AD7
P50	I/O	Port 5	Input	—
P51		8-bit I/O port		$\overline{\text{SCK}}$
P52		Input/output can be specified in 1-bit units.		SI
P53		LEDs can be driven directly.		SO
P54		An on-chip pull-up resistor can be specified by means of software.		INTP4/TI000/TO00
P55				INTP5/TI010
P56				INTP6/TI001/TO01
P57				INTP7/TI011
P64	I/O	Port 6	Input	$\overline{\text{RD}}$
P65		4-bit I/O port		$\overline{\text{WR}}$
P66		Input/output can be specified in 1-bit units.		$\overline{\text{WAIT}}$
P67		An on-chip pull-up resistor can be specified by means of software.		ASTB

2.2 Non-Port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P00/TOFF7
INTP1			Input	P01
INTP2			Input	P02
INTP3			Input	P03/ADTRG
INTP4			Input	P54/TI000/TO00
INTP5			Input	P55/TI010
INTP6			Input	P56/TI001/TO01
INTP7			Input	P57/TI011
TI50	Input	External count clock input to 8-bit timer (TM50)	Input	P24/TO50
TI51		External count clock input to 8-bit timer (TM51)	Input	P25/TO51
TI52		External count clock input to 8-bit timer (TM52)	Input	P26/TO52
TI000		External count clock input to 16-bit timer (TM00) Capture trigger input to capture register (CR000, CR010) of 16-bit timer (TM00)	Input	P54/INTP4/TO00
TI010		Capture trigger input to capture register (CR000) of 16-bit timer (TM00)	Input	P55/INTP5
TI001		External count clock input to 16-bit timer (TM01) Capture trigger input to capture register (CR001, CR011) of 16-bit timer (TM01)	Input	P56/INTP6/TO01
TI011		Capture trigger input to capture register (CR001) of 16-bit timer (TM01)	Input	P57/INTP7
TO50	Output	8-bit timer (TM50) output	Input	P24/TI50
TO51		8-bit timer (TM51) output	Input	P25/TI51
TO52		8-bit timer (TM52) output	Input	P26/TI52
TO00		16-bit timer (TM00) output	Input	P54/INTP4/TI000
TO01		16-bit timer (TM01) output	Input	P56/INTP6/TI001
RTP0 to RTP7	Output	Real-time output port that outputs pulses in synchronization with trigger signals outputs from the real-time pulse unit	Input	P30 to P37
TxD00	Output	Asynchronous serial interface serial data output	Input	P21
TxD01			Input	P23
RxD00	Input	Asynchronous serial interface serial data input	Input	P20
RxD01			Input	P22
$\overline{\text{SCK}}$	I/O	Serial interface serial clock input/output	Input	P51
SI	Input	Serial interface serial data input	Input	P52
SO	Output	Serial interface serial data output	Input	P53
ANI0 to ANI7	Input	A/D converter analog input	Input	P10 to P17
ADTRG	Input	External trigger signal input to the A/D converter	Input	P03/INTP3
TO70 to TO75	Output	Timer output for the 3-phase PWM inverter control	Hi-Z	–
TOFF7	Input	Timer output (TO70 to TO75) stop external input	Input	P00/INTP0
AD0 to AD7	I/O	Address/data bus for expanding memory externally	Input	P40 to P47
$\overline{\text{RD}}$	Output	Strobe signal output for reading from external memory	Input	P64
$\overline{\text{WR}}$		Strobe signal output for writing to external memory	Input	P65
$\overline{\text{WAIT}}$	Input	Wait insertion at external memory access	Input	P66
ASTB	Output	Strobe output that externally latches address information output to ports 4 and 5 to access external memory	Input	P67
AV$_{REF}$	Input	A/D converter reference voltage input	–	–
★ AV$_{DD}$	–	A/D converter analog power supply	–	–

2.2 Non-Port Pins (2/2)

★

| Pin Name	I/O	Function	After Reset	Alternate Function
AV$_{SS}$	–	A/D converter ground potential	–	–
$\overline{\text{RESET}}$	Input	System reset input	–	–
X1	Input	Connecting crystal resonator for system clock oscillation	–	–
X2	–		–	–
V$_{DD0}$	–	Positive power supply for ports	–	–
V$_{SS0}$	–	Ground potential for ports	–	–
V$_{DD1}$	–	Positive power supply except for ports	–	–
V$_{SS1}$	–	Ground potential except for ports	–	–
V$_{PP}$	–	High-voltage application during program write/verify. In the normal operation mode, connect directly to V$_{SS0}$.	–	–

★ **2.3 Pin I/O Circuits and Recommended Connection of Unused Pins**

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 2-1.

For the input/output circuit configuration of each type, refer to Figure 2-1.

Table 2-1. Types of Pin Input/Output Circuits

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection of Unused Pins
P00/INTP0/TOFF7	8-C	Input/output	Independently connect to V_{SS0} via a resistor.
P01/INTP1			
P02/INTP2			
P03/INTP3/ADTRG			
P10/ANI0 to P17/ANI7	25	Input	Independently connect to V_{DD0} or V_{SS0} via a resistor.
P20/RxD00	8-C	Input/output	
P21/TxD00	5-H		
P22/RxD01	8-C		
P23/TxD01	5-H		
P24/TI50/TO50	8-C		
P25/TI51/TO51			
P26/TI52/TO52			
P30/RTP0 to P37/RTP7	5-H		
P40/AD0 to P47/AD7			
P50			
P51/$\overline{SCK}$	8-C		
P52/SI	5-H		
P53/SO			
P54/INTP4/TI000/TO00			
P55/INTP5/TI010			
P56/INTP6/TI001/TO01			
P57/INTP7/TI011			
P64/$\overline{RD}$			
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			
TO70 to TO75	4	Output	Leave open.
$\overline{RESET}$	2	Input	–
AV_{DD}	–	–	Connect to V_{DD0}.
AV_{REF}			Connect to V_{SS0}.
AV_{SS}			
V_{PP}			Connect directly to V_{SS0}.

Figure 2-1. Pin Input/Output Circuits
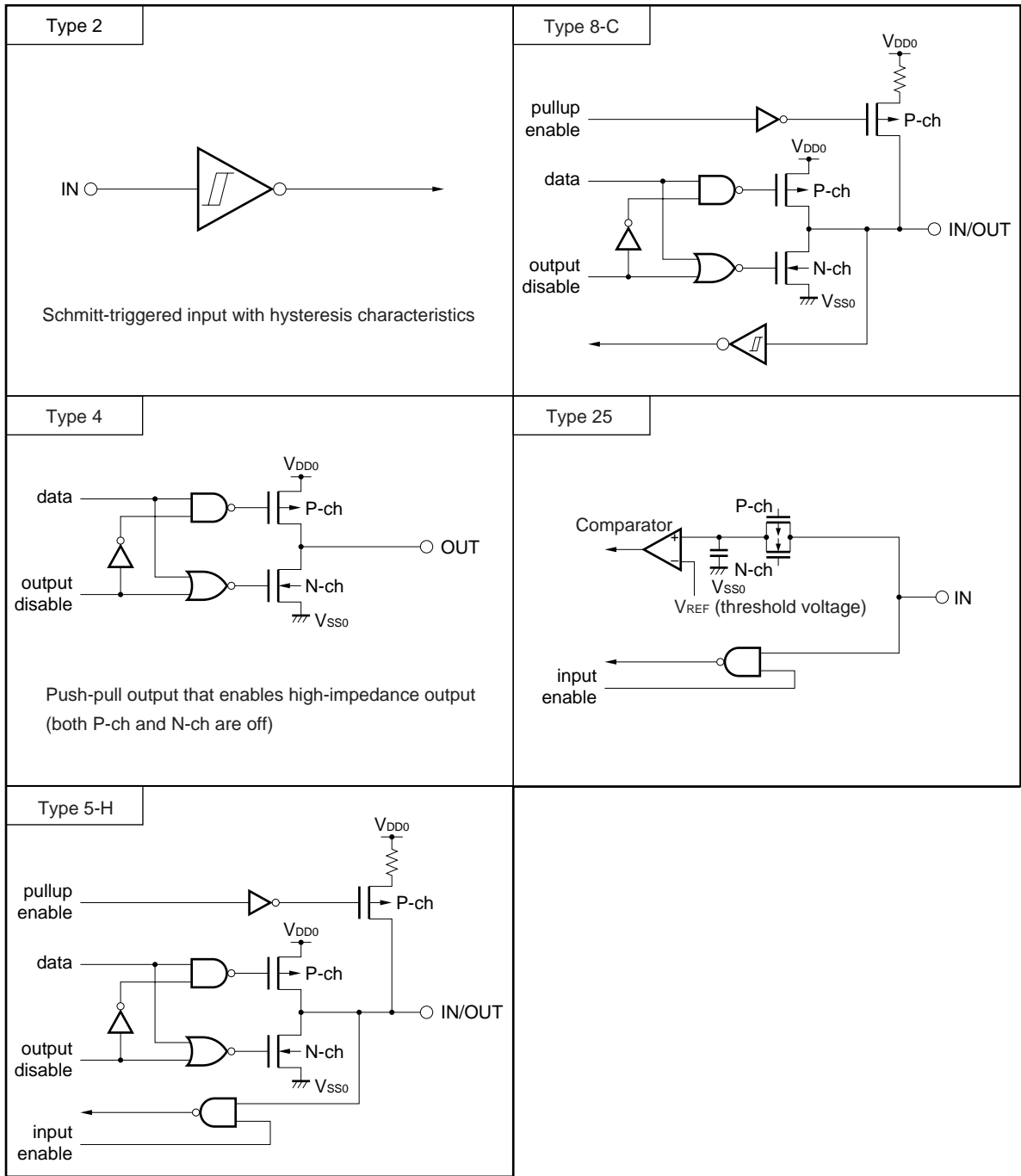
3. INTERNAL MEMORY SIZE SWITCHING REGISTER (IMS)

This register is set by software not to use a part of internal memory. The memory mapping can be made the same as that of mask ROM versions with different types of internal memory capacity by setting IMS.

IMS is set with an 8-bit memory manipulation instruction.

IMS is set to CFH by $\overline{\text{RESET}}$ input.

★ **Figure 3-1. Format of Internal Memory Size Switching Register**
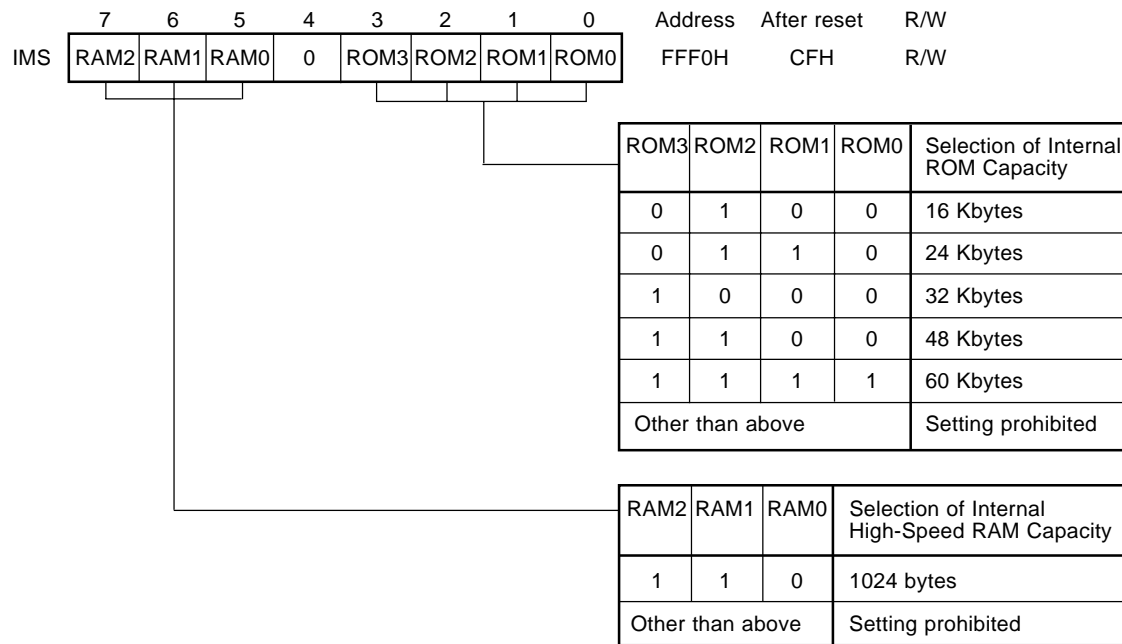

Table 3-1 shows the IMS setting values to make the memory mapping the same as those of mask ROM versions.

★ **Table 3-1. Setting Value of Internal Memory Size Switching Register**

Target Mask ROM Versions	IMS Setting Value
μPD780982	C4H
μPD780983	C6H
μPD780984	C8H
μPD780986	CCH
μPD780988	CFH

4. INTERNAL EXPANSION RAM SIZE SWITCHING REGISTER (IXS)

This register is used to set internal expansion RAM capacity by software. The memory mapping can be made the same as that of mask ROM versions with different types of internal expansion RAM capacity by setting IXS.

IXS is set with an 8-bit memory manipulation instruction.

IXS is set to 0CH by $\overline{\text{RESET}}$ input.

Figure 4-1. Format of Internal Expansion RAM Size Switching Register

	7	6	5	4	3	2	1	0	Address	After reset	R/W
IXS	0	0	0	IXRAM4	IXRAM3	IXRAM2	IXRAM1	IXRAM0	FFF4H	0CH	R/W

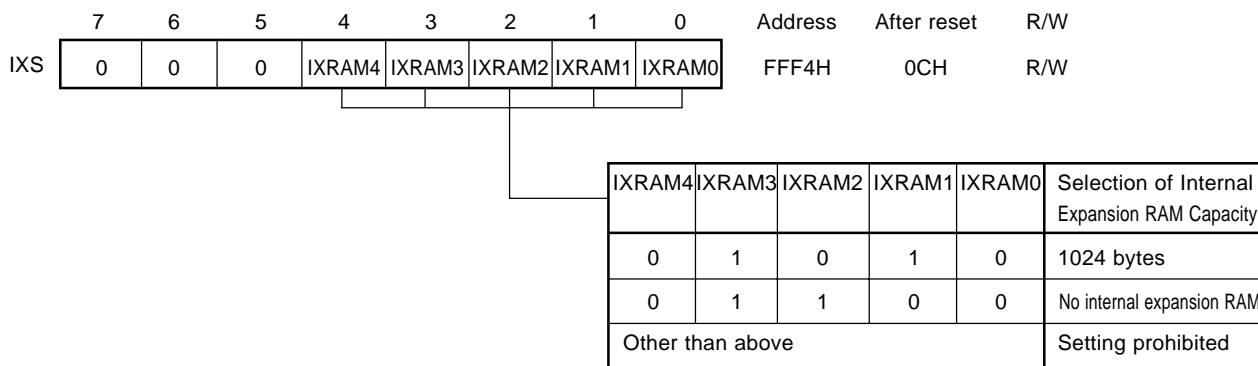| IXRAM4	IXRAM3	IXRAM2	IXRAM1	IXRAM0	Selection of Internal Expansion RAM Capacity
0	1	0	1	0	1024 bytes
0	1	1	0	0	No internal expansion RAM
Other than above					Setting prohibited

Table 4-1 shows the IXS setting values to make the memory mapping the same as those of mask ROM versions.

★   **Table 4-1. Setting Value of Internal Expansion RAM Size Switching Register**

Target Mask ROM Versions	IXS Setting Value
*μ*PD780982	0CH
*μ*PD780983	
*μ*PD780984	
*μ*PD780986	0AH
*μ*PD780988	

5. FLASH MEMORY PROGRAMMING

On-board writing of flash memory (with device mounted on target system) is supported. On-board writing is done
★ after connecting a dedicated flash programmer (Flashpro II (part number FL-PR2), Flashpro III (part numbers FL-PR3
and PG-FP3)) to the host machine and target system. Moreover, writing to flash memory can also be performed using
a flash memory writing adapter connected to Flashpro II or Flashpro III.

★ **Remark**   FL-PR2 and FL-PR3 are products of NAITO DENSEI MACHIDA MFG. CO., LTD.

5.1   Selection of Communication Mode

Writing to flash memory is performed using Flashpro II and III with a serial communication mode. Select the
communication mode for writing from Table 5-1. For the selection of the communication mode, a format like the one
shown in Figure 5-1 is used. The communication modes are selected using the V_{PP} pulse numbers shown in Table
5-1.

Table 5-1. Communication Mode List

Communication Mode	Number of Channels	Pin Used	Number of V_{PP} Pulses
3-wire serial I/O	1	$\overline{SCK}$/P51 SI/P52 SO/P53	0
UART	1	RxD00/P20 TxD00/P21	8
Pseudo 3-wire serial I/O mode[Note]	1	P24/TI50/TO50 (Serial data input) P25/TI51/TO51 (Serial data output) P26/TI52/TO52 (Serial clock input)	12

Note   Serial transfer is performed by controlling ports with software.

**Caution   Always select the communication mode according to the number of V_{PP} pulses shown in Table 5-
1.**

Figure 5-1. Communication Mode Selection Format
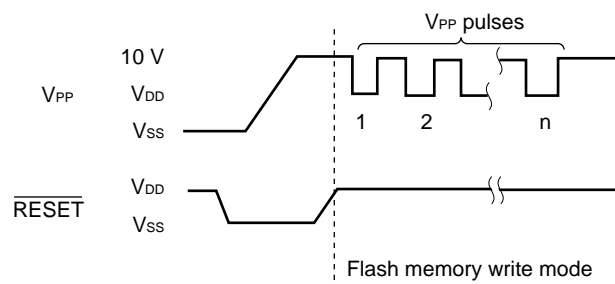
5.2 Flash Memory Programming Functions

Flash memory writing is performed through command and data transmit/receive operations using the selected communication mode. The main functions are listed in Table 5-2.

Table 5-2. Main Functions of Flash Memory Programming

Function	Description
Batch erase	Erases the contents of the entire memory.
Batch blank check	Checks that the entire memory has been deleted.
Data write	Performs writing to flash memory according to the write start address and the number of the data to be written (the number of bytes).
Batch verify	Compares the contents of the entire memory and the input data.

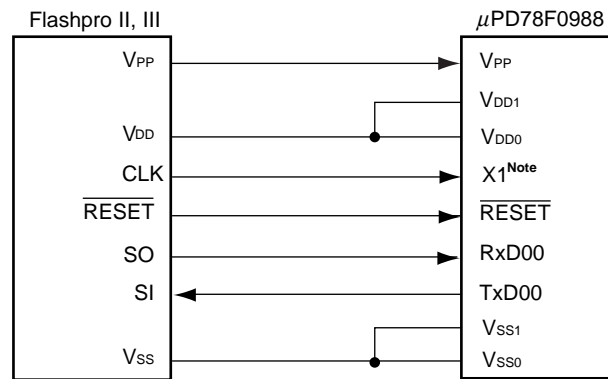### 5.3 Connection of Flashpro II and Flashpro III

The connection of the Flashpro II, Flashpro III and the μPD78F0988 differs depending on the communication mode. Each type of connection is shown in Figures 5-2, 5-3, and 5-4, respectively.

★ **Figure 5-2. Connection of Flashpro II and Flashpro III Using 3-Wire Serial I/O Mode**
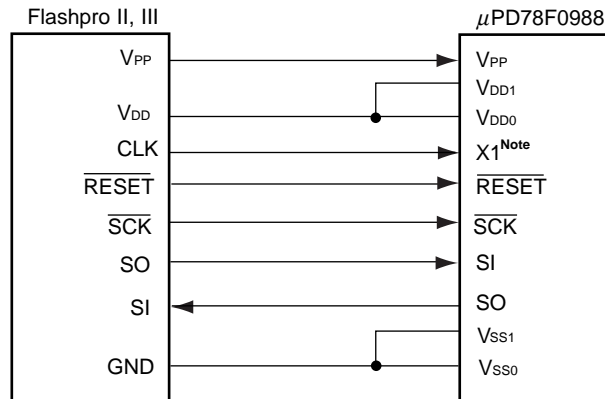
Note For input to X1, not CLK but a normal oscillator can also be used.

Figure 5-3. Connection of Flashpro II and Flashpro III Using UART Mode

Note For input to X1, not CLK but a normal oscillator can also be used.

★ **Figure 5-4. Connection of Flashpro II and Flashpro III Using Pseudo 3-Wire Serial I/O Mode**
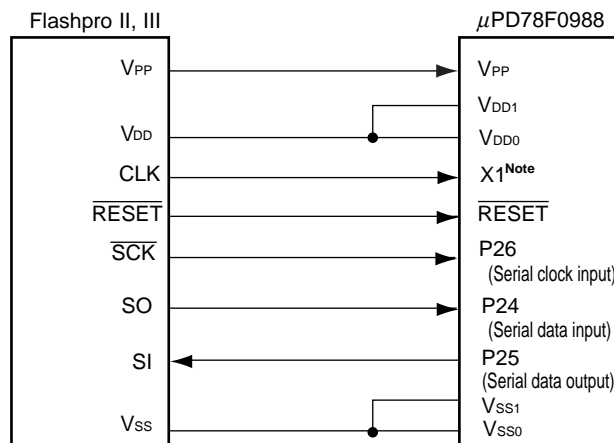
Note For input to X1, not CLK but a normal oscillator can also be used.

★ **6. ELECTRICAL SPECIFICATIONS**

Absolute Maximum Ratings (T$_A$ = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V$_{DD}$			−0.3 to +6.5	V
	V$_{PP}$			−0.3 to +10.5	V
	AV$_{DD}$			−0.3 to V$_{DD}$ + 0.3	V
	AV$_{REF}$			−0.3 to V$_{DD}$ + 0.3	V
	AV$_{SS}$			−0.3 to +0.3	V
Input voltage	V$_I$	P00 to P03, P10 to P17, P20 to P26, P30 to P37, P50 to P57, P64 to P67, TO70 to TO75, X1, X2, $\overline{\text{RESET}}$		−0.3 to V$_{DD}$ + 0.3	V
Output voltage	V$_O$			−0.3 to V$_{DD}$ + 0.3	V
Analog input voltage	V$_{AN}$	P10 to P17	Analog input pin	AV$_{SS}$ − 0.3 to AV$_{REF}$ + 0.3 and −0.3 to V$_{DD}$ + 0.3	V
Output current, high	I$_{OH}$	Per pin		−10	mA
		P00, P01, P30 to P37, P40 to P47, P50 to P57, P64 to P67 total		−15	mA
		P02, P03, P20 to P26, TO70 to TO75 total		−15	mA
Output current, low	I$_{OL}$**Note**	P00 to P03, P10 to P17, P20 to P26, P30 to P37, P40 to P47, P64 to P67 per pin	Peak value	20	mA
			rms value	10	mA
		P50 to P57, TO70 to TO75 per pin	Peak value	30	mA
			rms value	15	mA
		P00, P01, P30 to P37, P40 to P47, P64 to P67 total	Peak value	50	mA
			rms value	20	mA
		P02, P03, P20 to P26 total	Peak value	30	mA
			rms value	15	mA
		TO70 to TO75 total	Peak value	100	mA
			rms value	70	mA
		P50 to P57 total	Peak value	100	mA
			rms value	70	mA
Operating ambient temperature	T$_A$			−40 to +85	$^\circ$C
Storage temperature	T$_{stg}$			−40 to +125	$^\circ$C

Note The rms value should be calculated as follows: [rms value] = [Peak value] $\times \sqrt{\text{Duty}}$

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Capacitance (T$_A$ = 25°C, V$_{DD}$ = V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C$_{IN}$	f = 1 MHz Unmeasured pins returned to 0 V				15	pF
I/O capacitance	C$_{IO}$	f = 1 MHz Unmeasured pins returned to 0 V	P00 to P03, P20 to P26, P30 to P37, P40 to P47, P50 to P57, P64 to P67, TO70 to TO75			15	pF

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

System Clock Oscillator Characteristics (T$_A$ = –40 to +85°C, V$_{DD}$ = 4.0 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator	V$_{PP}$ X2 X1 C1 C2	Oscillation frequency (f$_X$)[Note 1]		1.0		8.38	MHz
		Oscillation stabilization time[Note 2]	After V$_{DD}$ reaches oscillation voltage range MIN.			4	ms
Crystal resonator	V$_{PP}$ X2 X1 C1 C2	Oscillation frequency (f$_X$)[Note 1]		1.0		8.38	MHz
		Oscillation stabilization time[Note 2]	After V$_{DD}$ reaches oscillation voltage range MIN.			10	ms
External clock	X2 X1 μPD74HCU04	X1 input frequency (f$_X$)[Note 1]		1.0		8.38	MHz
		X1 input high-/low-level width (t$_{XH}$, t$_{XL}$)		50		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release.

Caution When using the system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V$_{SS1}$.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

Recommended Oscillator Constant

System clock: Ceramic resonator (T$_A$ = –40 to +85°C)

Manufacturer	Part Number	Frequency (MHz)	Recommended Circuit Constant		Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
Murata Mfg. Co., Ltd.	CSA2.00MG040	2.00	100	100	4.0	5.5
	CST2.00MG040	2.00	On-chip	On-chip	4.0	5.5
	CSA3.58MG	3.58	30	30	4.0	5.5
	CST3.58MGW	3.58	On-chip	On-chip	4.0	5.5
	CSA4.00MG	4.00	30	30	4.0	5.5
	CST4.00MGW	4.00	On-chip	On-chip	4.0	5.5
	CSA4.19MG	4.19	30	30	4.0	5.5
	CST4.19MGW	4.19	On-chip	On-chip	4.0	5.5
	CSA4.91MG	4.91	30	30	4.0	5.5
	CST4.91MGW	4.91	On-chip	On-chip	4.0	5.5
	CSA5.00MG	5.00	30	30	4.0	5.5
	CST5.00MGW	5.00	On-chip	On-chip	4.0	5.5
	CSA7.37MTZ	7.37	30	30	4.0	5.5
	CST7.37MTW	7.37	On-chip	On-chip	4.0	5.5
	CSA8.00MTZ	8.00	30	30	4.0	5.5
	CST8.00MTW	8.00	On-chip	On-chip	4.0	5.5
	CSA8.38MTZ	8.38	30	30	4.0	5.5
	CST8.38MTW	8.38	On-chip	On-chip	4.0	5.5
	CSA10.0MTZ	10.0	30	30	4.0	5.5
	CST10.0MTW	10.0	On-chip	On-chip	4.0	5.5

Caution   The oscillator constant and oscillation voltage range indicate conditions of stable oscillation. Oscillation frequency precision is not guaranteed. For applications requiring oscillation frequency precision, the oscillation frequency must be adjusted on the implementation circuit. For details, please contact directly the manufacturer of the resonator you will use.

DC Characteristics (T$_A$ = –40 to +85°C, V$_{DD}$ = 4.0 to 5.5 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input voltage, high	V$_{IH1}$	P10 to P17, P21, P23, P30 to P37, P40 to P47, P50, P53, P64 to P67			0.7V$_{DD}$		V$_{DD}$	V
	V$_{IH2}$	$\overline{\text{RESET}}$, P00 to P03, P20, P22, P24 to P26, P51, P52, P54 to P57			0.8V$_{DD}$		V$_{DD}$	V
	V$_{IH3}$	X1, X2			V$_{DD}$ – 0.5		V$_{DD}$	V
Input voltage, low	V$_{IL1}$	P10 to P17, P21, P23, P30 to P37, P40 to P47, P50, P53, P67			0		0.3V$_{DD}$	V
	V$_{IL2}$	$\overline{\text{RESET}}$, P00 to P03, P20, P22, P24 to P26, P51, P52, P54 to P57			0		0.2V$_{DD}$	V
	V$_{IL3}$	X1, X2			0		0.4	V
Output voltage, high	V$_{OH1}$	4.5 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OH}$ = –1 mA			V$_{DD}$ – 1.0		V$_{DD}$	V
		I$_{OH}$ = –100 μA			V$_{DD}$ – 0.5		V$_{DD}$	V
Output voltage, low	V$_{OL1}$	P50 to P57, TO70 to TO75	5.0 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL}$ = 15 mA			0.4	2.0	V
		P00 to P03, P20 to P26, P30 to P37, P40 to P47, P64 to P67	5.0 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL}$ = 1.6 mA				0.4	V
	V$_{OL2}$	I$_{OL}$ = 400 μA					0.5	V
Input leakage current, high	I$_{LIH1}$	V$_{IN}$ = V$_{DD}$	P00 to P03, P10 to P17, P20 to P26, P30 to P37, P40 to P47, P50 to P57, P64 to P67, TO70 to TO75, $\overline{\text{RESET}}$				3	μA
	I$_{LIH2}$		X1, X2				20	μA
Input leakage current, low	I$_{LIL1}$	V$_{IN}$ = 0 V	P00 to P03, P10 to P17, P20 to P26, P30 to P37, P40 to P47, P50 to P57, P64 to P67, TO70 to TO75, $\overline{\text{RESET}}$				–3	μA
	I$_{LIL2}$		X1, X2				–20	μA
Output leakage current, high	I$_{LOH}$	V$_{OUT}$ = V$_{DD}$					3	μA
Output leakage current, low	I$_{LOL}$	V$_{OUT}$ = 0 V					–3	μA
Software pull-up resistor	R$_2$	V$_{IN}$ = 0 V P00 to P03, P20 to P26, P30 to P37, P40 to P47, P50 to P57, P64 to P67			15	30	90	kΩ
Power supply current[Note 1]	I$_{DD1}$	8.38-MHz crystal oscillation operating mode	V$_{DD}$ = 5.0 V ±10%[Note 2]	When A/D converter stopped		15	30	mA
				When A/D converter operating		16	32	mA
	I$_{DD2}$	8.38-MHz crystal oscillation HALT mode	V$_{DD}$ = 5.0 V ±10%[Note 2]	When peripheral function stopped		1.3	2.6	mA
				When peripheral function operating			7.3	mA
	I$_{DD3}$	STOP mode	V$_{DD}$ = 5.0 V ±10%			0.1	30	μA

Notes 1. Refers to the total current flowing to the internal power supply (V$_{DD0}$ and V$_{DD1}$). The peripheral operation current is included however, the current flowing to the pull-up resistor of ports and AV$_{REF}$ pin is not included.

2. High-speed mode operation (when processor clock control register (PCC) is set to 00H).

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

AC Characteristics

(1) Basic operation (T$_A$ = −40 to +85°C, V$_{DD}$ = 4.0 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T$_{CY}$	Operating with system clock	0.24		32	μs
TI000, TI001, TI010, TI011 input frequency	f$_{TI0}$		0		f$_X$/64	MHz
TI000, TI001, TI010, TI011 input high-/ low-level width	t$_{TIH0}$ t$_{TIL0}$		2/f$_{sam}$ + 0.1**Note**			μs
TI50, TI51, TI52 input frequency	f$_{TI5}$	8-/16-bit precision	0		4	MHz
TI50, TI51, TI52 input high-/ low-level width	t$_{TIH5}$ t$_{TIL5}$	8-/16-bit precision	100			ns
Interrupt request input high-/ low-level width	t$_{INTH}$ t$_{INTL}$	INTP0 to INTP7	1			μs
TOFF input high-/low-level width	t$_{TOFFH}$ t$_{TOFFL}$		2			μs
$\overline{\text{RESET}}$ input low-level width	t$_{RSL}$		10			μs

Note Selection of f$_{sam}$ = f$_X$, f$_X$/4, f$_X$/32 is possible with bits 0 and 1 (PRM000, PRM001) of prescaler mode register 00 (PRM00) or with bits 0 and 1 (PRM010, PRM011) of prescaler mode register 01 (PRM01). Note that when selecting TI000 (TM00) or TI001 (TM01) valid edge as the count clock, f$_{sam}$ = f$_X$/16.

TCY **vs V**DD **(System clock operation)**

Supply voltage VDD [V]
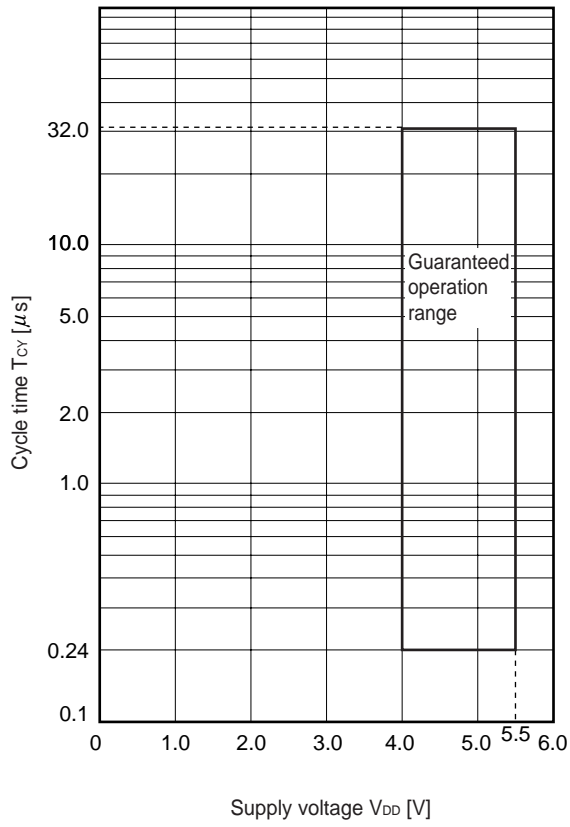
(2) Read/write operation (T$_A$ = –40 to +85°C, V$_{DD}$ = 4.0 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t$_{ASTH}$		0.3t$_{CY}$		ns
Address setup time	t$_{ADS}$		20		ns
Address hold time	t$_{ADH}$		6		ns
Data input time from address	t$_{ADD1}$			(2 + 2n)t$_{CY}$ − 54	ns
	t$_{ADD2}$			(3 + 2n)t$_{CY}$ − 60	ns
Address output time from $\overline{RD}\downarrow$	t$_{RDAD}$		0	100	ns
Data input time from $\overline{RD}\downarrow$	t$_{RDD1}$			(2 + 2n)t$_{CY}$ − 87	ns
	t$_{RDD2}$			(3 + 2n)t$_{CY}$ − 93	ns
Read data hold time	t$_{RDH}$		0		ns
$\overline{RD}$ low-level width	t$_{RDL1}$		(1.5 + 2n)t$_{CY}$ − 33		ns
	t$_{RDL2}$		(2.5 + 2n)t$_{CY}$ − 33		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	t$_{RDWT1}$			t$_{CY}$ − 43	ns
	t$_{RDWT2}$			t$_{CY}$ − 43	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	t$_{WRWT}$			0.5t$_{CY}$ − 25	ns
$\overline{WAIT}$ low-level width	t$_{WTL}$		(0.5 + 2n)t$_{CY}$ + 10	(2 + 2n)t$_{CY}$	ns
Write data setup time	t$_{WDS}$		60		ns
Write data hold time	t$_{WDH}$		6		ns
$\overline{WR}$ low-level width	t$_{WRL}$		(1.5 + 2n)t$_{CY}$ − 15		ns
$\overline{RD}\downarrow$ delay time from ASTB$\downarrow$	t$_{ASTRD}$		6		ns
$\overline{WR}\downarrow$ delay time from ASTB$\downarrow$	t$_{ASTWR}$		2t$_{CY}$ − 15		ns
ASTB$\uparrow$ delay time from $\overline{RD}\uparrow$ at external fetch	t$_{RDAST}$		0.8t$_{CY}$ − 15	1.2t$_{CY}$	ns
Write data output time from $\overline{RD}\uparrow$	t$_{RDWD}$		40		ns
Write data output time from $\overline{WR}\downarrow$	t$_{WRWD}$		10	60	ns
$\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t$_{WTRD}$		0.8t$_{CY}$	2.5t$_{CY}$ + 25	ns
$\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t$_{WTWR}$		0.8t$_{CY}$	2.5t$_{CY}$ + 25	ns

Remarks **1.** t$_{CY}$ = T$_{CY}$/4

2. n indicates the number of waits.

3. C$_L$ = 100 pF (C$_L$ is the load capacitance of AD0 to AD7, $\overline{RD}$, $\overline{WR}$, $\overline{WAIT}$, and ASTB pins.)

(3) Serial interface (T$_A$ = –40 to +85°C, V$_{DD}$ = 4.0 to 5.5 V)

(a) 3-wire serial I/O mode ($\overline{SCK}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t$_{KCY1}$		954			ns
$\overline{SCK}$ high-/low-level width	t$_{KH1}$ t$_{KL1}$		t$_{KCY1}$/2 − 50			ns
SI setup time (to $\overline{SCK}$↑)	t$_{SIK1}$		100			ns
SI hold time (from $\overline{SCK}$↑)	t$_{KSI1}$		400			ns
SO output delay time from $\overline{SCK}$↓	t$_{KSO1}$	C = 100 pF**Note**			300	ns

Note C is the load capacitance of the $\overline{SCK}$ and SO output lines.

(b) 3-wire serial I/O mode ($\overline{SCK}$... External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t$_{KCY2}$		800			ns
$\overline{SCK}$ high-/low-level width	t$_{KH2}$ t$_{KL2}$		400			ns
SI setup time (to $\overline{SCK}$↑)	t$_{SIK2}$		100			ns
SI hold time (from $\overline{SCK}$↑)	t$_{KSI2}$		400			ns
SO output delay time from $\overline{SCK}$↓	t$_{KSO2}$	C = 100 pF**Note**			300	ns

Note C is the load capacitance of the $\overline{SCK}$ and SO output lines.

(c) UART mode (UART00) (Dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					125000	bps

(d) UART mode (UART00) (Infrared data transfer mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					115200	bps
Bit rate allowable error					±0.87	%
Output pulse width			1.2		0.24/fbr**Note**	μs
Input pulse width			4/f$_X$			μs

Note fbr: Set baud rate

(e) UART mode (UART01) (Dedicated baud rate generator output)

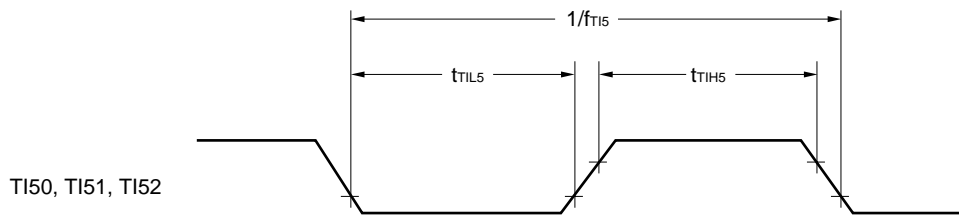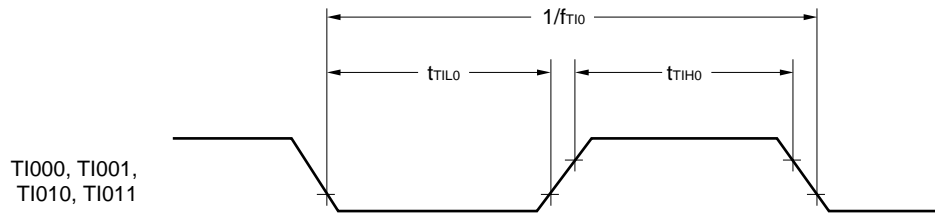| Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					38400	bps

AC Timing Test Points (excluding X1 input)

0.8V_{DD}		

0.8V$_{DD}$ Test points 0.8V$_{DD}$
0.2V$_{DD}$ 0.2V$_{DD}$

Clock Timing

1/f$_X$

t$_{XL}$ t$_{XH}$

X1 input V$_{IH3}$ (MIN.) / V$_{IL3}$ (MAX.)

TI Timing

1/f$_{TI0}$

t$_{TIL0}$ t$_{TIH0}$

TI000, TI001, TI010, TI011

1/f$_{TI5}$

t$_{TIL5}$ t$_{TIH5}$

TI50, TI51, TI52

TOFF Timing

t$_{TOFFL}$ t$_{TOFFH}$

TOFF7
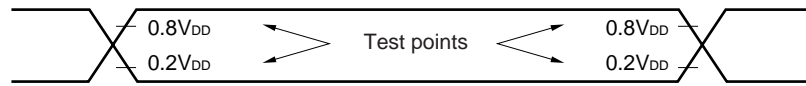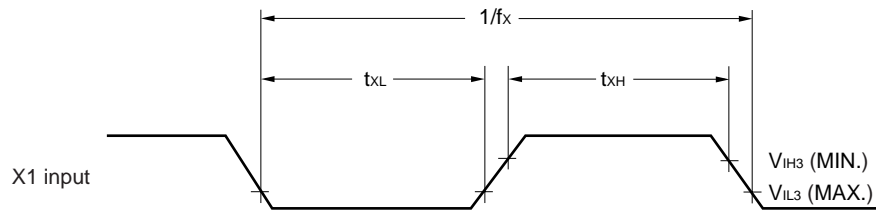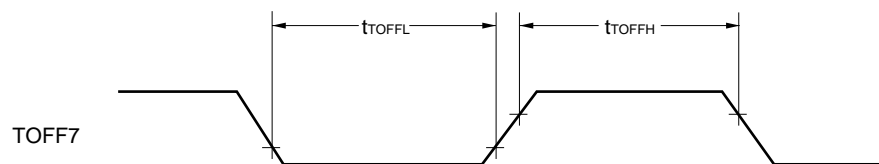
Read/Write Operation

External fetch (no wait):
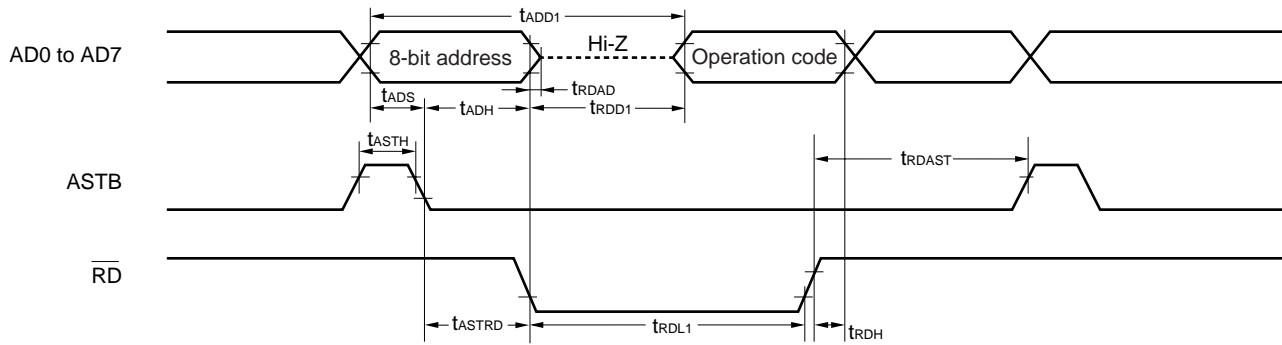
External fetch (wait insertion):
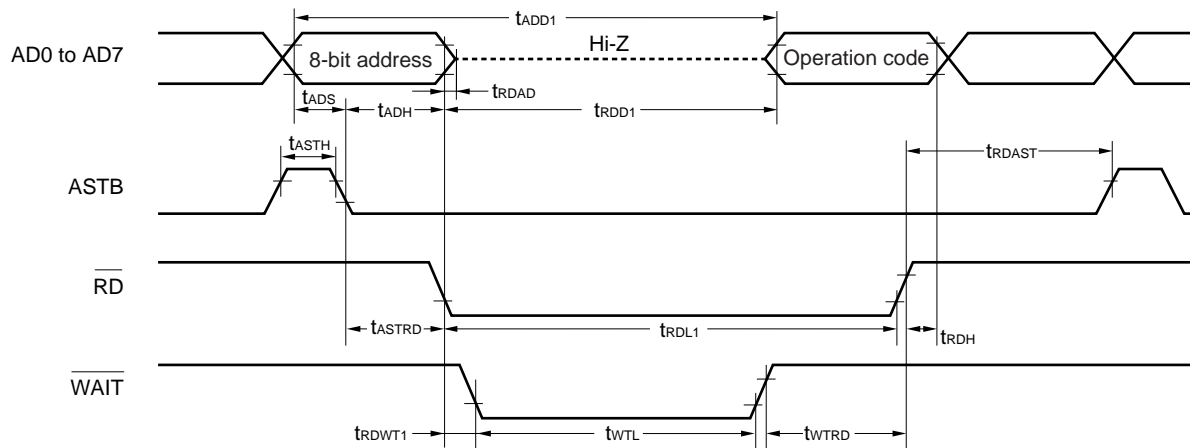
External data access (no wait):
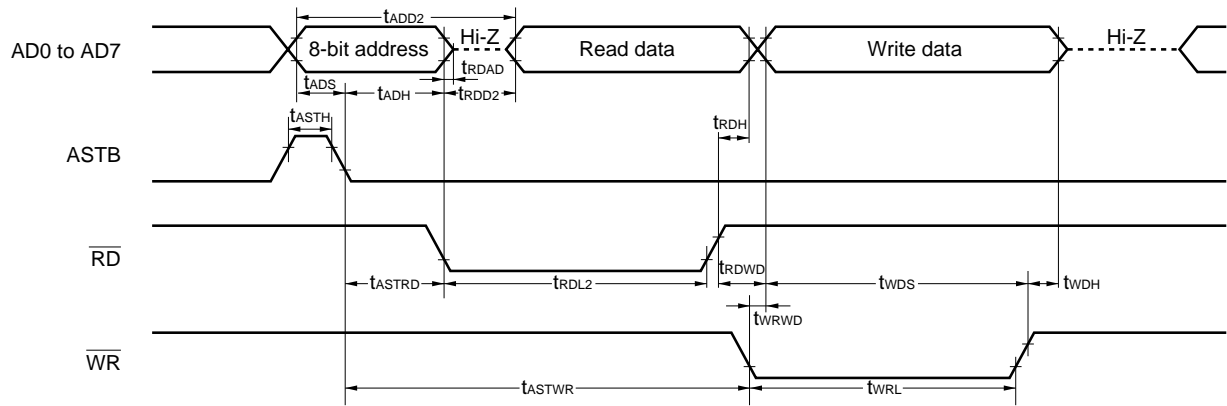
External data access (wait insertion):
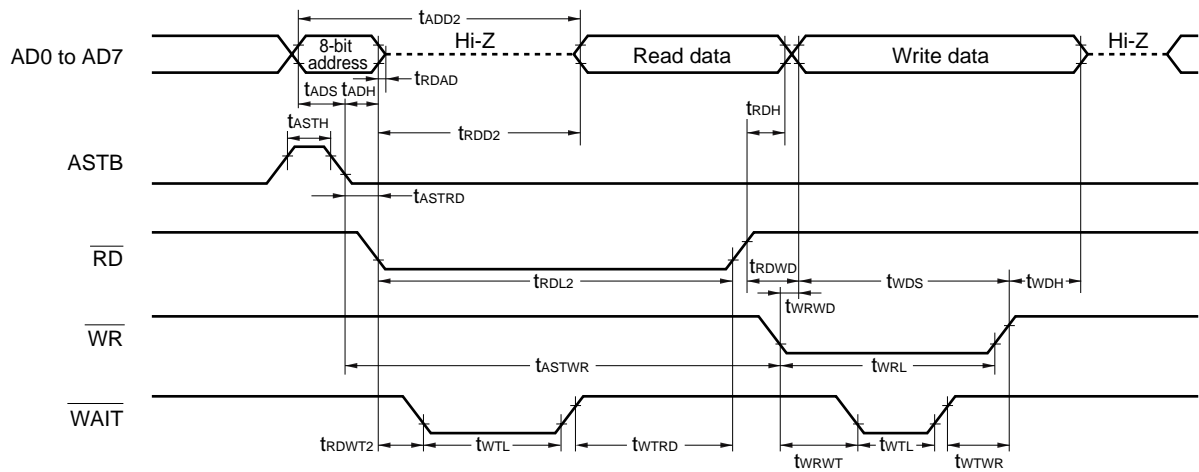
Serial Transfer Timing

3-wire serial I/O mode:
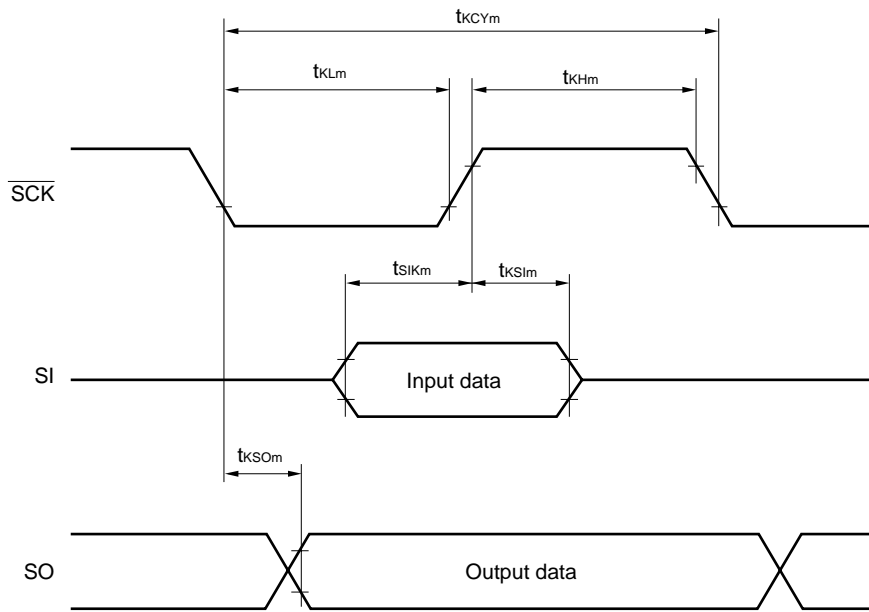
m = 1, 2

A/D Converter Characteristics (T$_A$ = –40 to +85°C, V$_{DD}$ = AV$_{DD}$ = 4.0 to 5.5 V, AV$_{SS}$ = V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error**Note**		4.0 V ≤ AV$_{REF}$ ≤ 5.5 V		±0.2	±0.4	%FSR
		2.7 V ≤ AV$_{REF}$ < 4.0 V		±0.3	±0.6	%FSR
Conversion time	t$_{CONV}$	4.0 V ≤ AV$_{REF}$ ≤ 5.5 V	14		96	μs
		2.7 V ≤ AV$_{REF}$ < 4.0 V	19		96	μs
Zero-scale offset**Note**		4.0 V ≤ AV$_{REF}$ ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV$_{REF}$ < 4.0 V			±0.6	%FSR
Full-scale offset**Note**		4.0 V ≤ AV$_{REF}$ ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV$_{REF}$ < 4.0 V			±0.6	%FSR
Non-linearity error		4.0 V ≤ AV$_{REF}$ ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ AV$_{REF}$ < 4.0 V			±4.5	LSB
Differential non-linearity error		4.0 V ≤ AV$_{REF}$ ≤ 5.5 V			±1.5	LSB
		2.7 V ≤ AV$_{REF}$ < 4.0 V			±2.0	LSB
Analog input voltage	V$_{IAN}$		0		AV$_{REF}$	V
Reference voltage	AV$_{REF}$		2.7		AV$_{DD}$	V
Resistance between AV$_{REF}$ and AV$_{SS}$	R$_{REF}$	When A/D converter is not operating	20	40		kΩ

Note Excludes quantization error (±1/2 LSB). It is indicated as a ratio to the full-scale value.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T$_A$ = –40 to +85°C)
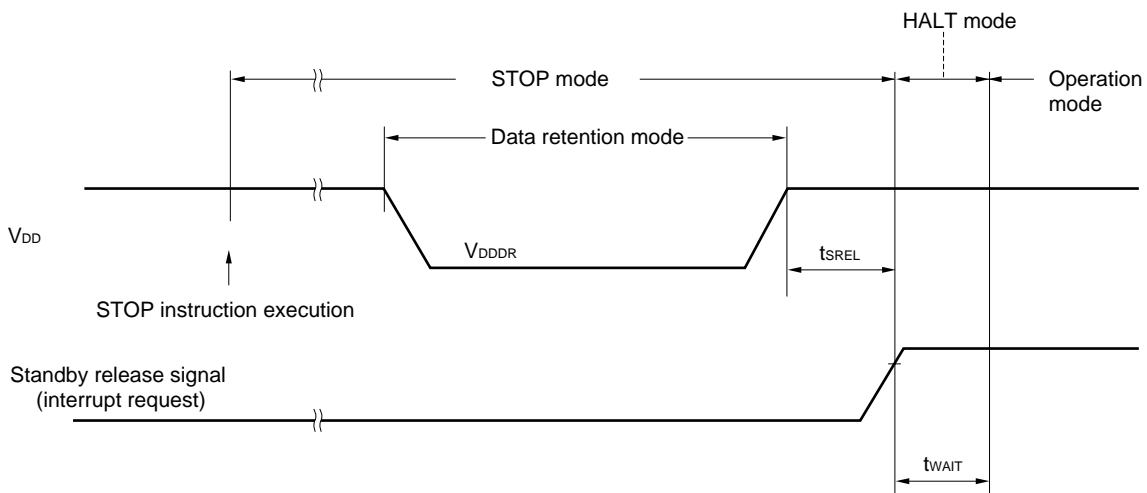
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V$_{DDDR}$		2.0		5.5	V
Data retention power supply current	I$_{DDDR}$	V$_{DDDR}$ = 2.0 V		0.1	10	μA
Release signal set time	t$_{SREL}$		0			μs
Oscillation stabilization wait time	t$_{WAIT}$	Release by $\overline{\text{RESET}}$		$2^{17}/f_X$		ms
		Release by interrupt request		**Note**		ms

Note Selection of $2^{12}/f_X$ and $2^{14}/f_X$ to $2^{17}/f_X$ is possible with bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).
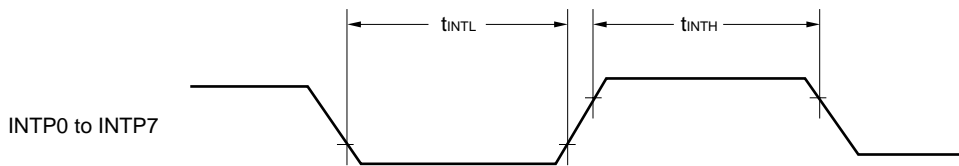
**Data Retention Timing (STOP mode release by $\overline{\text{RESET}}$)**

Internal reset operation

HALT mode

STOP mode

Operation mode

Data retention mode

V_{DD}

V_{DDDR}

t_{SREL}

STOP instruction execution

$\overline{\text{RESET}}$

t_{WAIT}
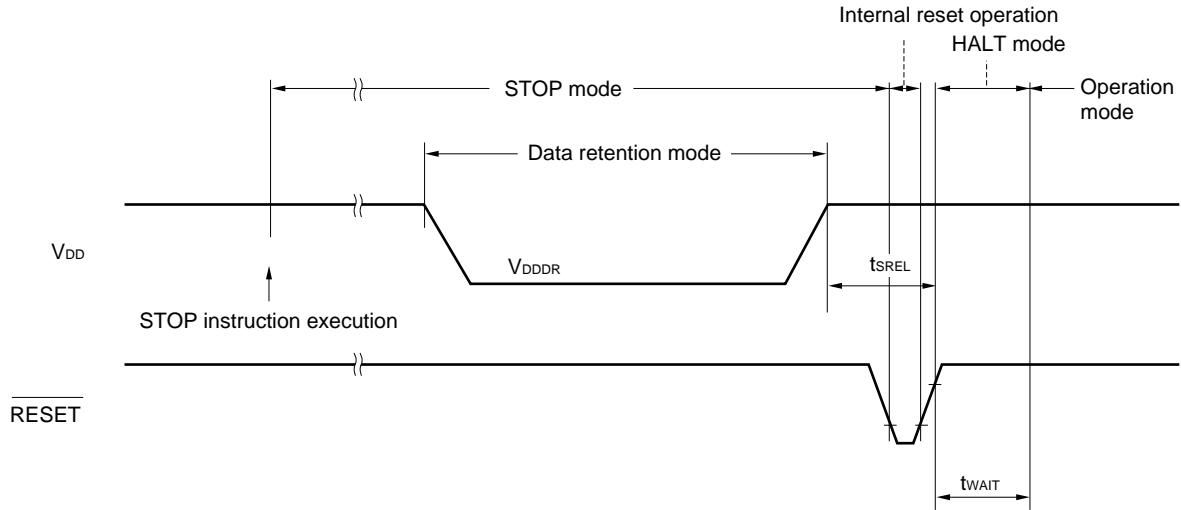
Data Retention Timing (Standby release signal: STOP mode release by interrupt request signal)

HALT mode

STOP mode

Operation mode

Data retention mode

V_{DD}

V_{DDDR}

t_{SREL}

STOP instruction execution

Standby release signal (interrupt request)

t_{WAIT}

Interrupt Request Input Timing

t_{INTL}

t_{INTH}

INTP0 to INTP7

$\overline{\text{RESET}}$ Input Timing

t_{RSL}

$\overline{\text{RESET}}$
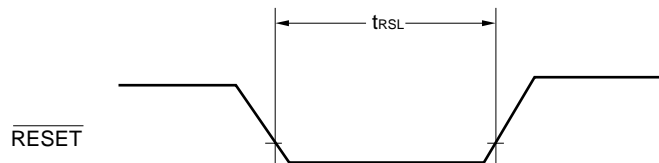
Flash Memory Programming Characteristics (V$_{DD}$ = 4.0 to 5.5 V, V$_{SS}$ = 0 V, V$_{PP}$ = 9.7 to 10.3 V)

(1) Basic characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operation frequency	f$_X$		1.0		8.38	MHz
Supply voltage	V$_{DD}$		4.0		5.5	V
	V$_{PPL}$	When V$_{PP}$ low-level is detected	0		0.2V$_{DD}$	V
	V$_{PP}$	When V$_{PP}$ high-level is detected	0.8V$_{DD}$	V$_{DD}$	1.2V$_{DD}$	V
	V$_{PPH}$	When V$_{PP}$ high-voltage is detected	9.0	10.0	10.5	V
		When programming	9.7	10.0	10.3	V
V$_{PP}$ power supply current	I$_{PP}$	V$_{PP}$ = 10.0 V		50	100	mA
Write time (per 1 byte)	T$_{WRT}$		50		500	μs
Number of rewrites	C$_{WRT}$				20	Times
Erase time	T$_{ERASE}$		1		20	s
Programming temperature	T$_{PRG}$		10		40	°C

(2) Serial write operation characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V$_{PP}$↑ set time from V$_{DD}$↑	t$_{DRPSR}$	V$_{PP}$ high voltage	0			μs
$\overline{RESET}$↑ set time from V$_{PP}$↑	t$_{PSRRF}$	V$_{PP}$ high voltage	1.0			μs
V$_{PP}$ count start time from $\overline{RESET}$↑	t$_{RFCF}$	V$_{PP}$ high voltage	1.0			μs
Count execution time	t$_{COUNT}$				20	ms
V$_{PP}$ counter high-level width	t$_{CH}$		8.0			μs
V$_{PP}$ counter low-level width	t$_{CL}$		8.0			μs
V$_{PP}$ counter noise elimination width	t$_{NFW}$			40		ns

Flash Write Mode Setting Timing
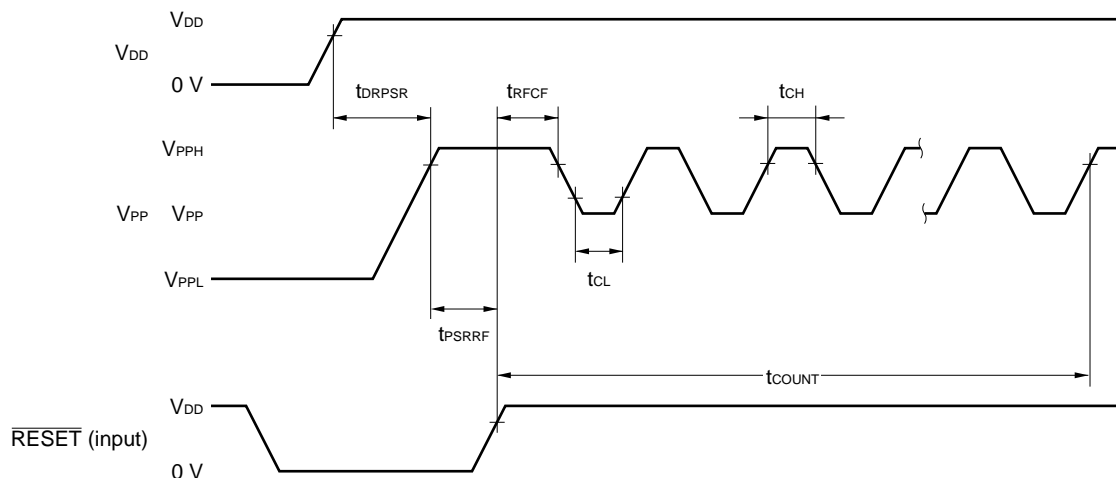
★ 7. PACKAGE DRAWINGS
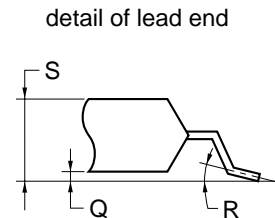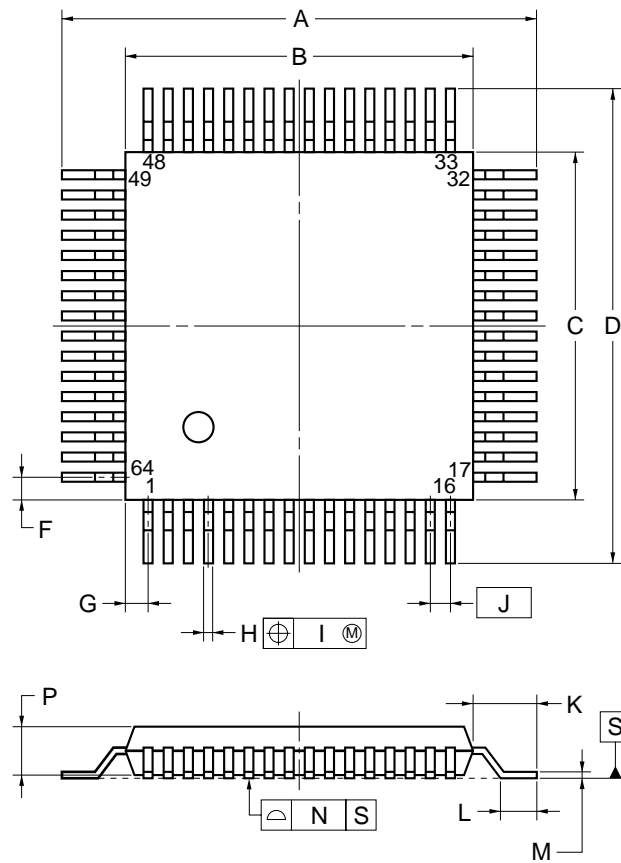
64 PIN PLASTIC SHRINK DIP (750 mil)
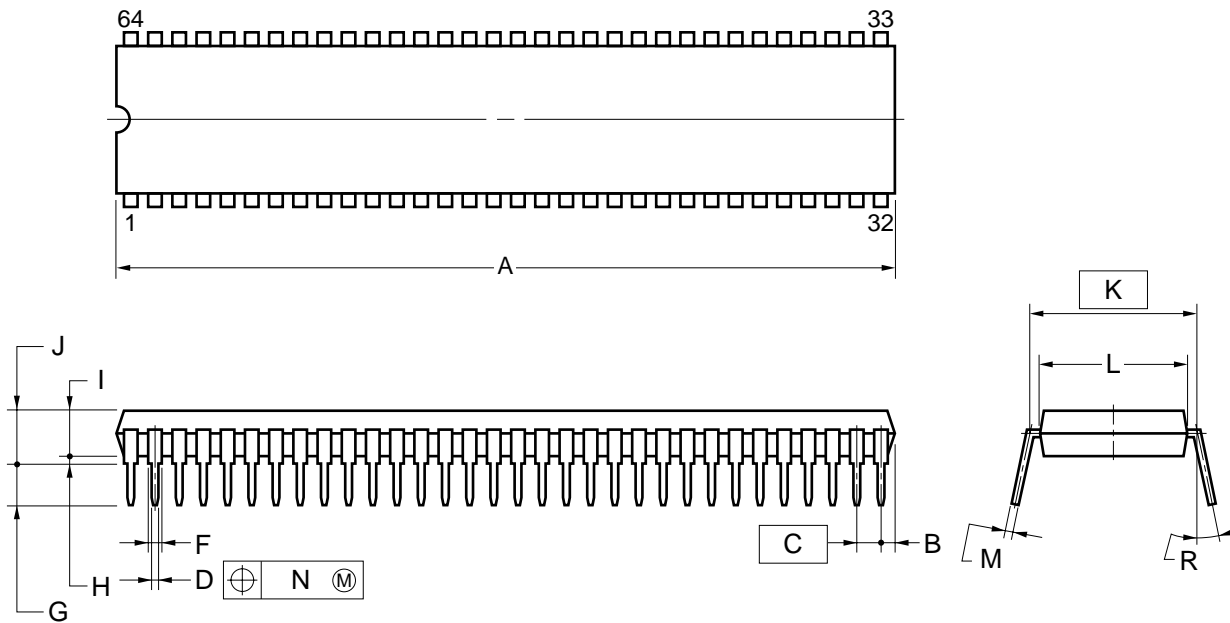
NOTES

1. Controlling dimension——— millimeter.

2. Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

3. Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	$58.0^{+0.68}_{-0.20}$	$2.283^{+0.028}_{-0.008}$
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2 ± 0.3	0.126 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	$4.05^{+0.26}_{-0.20}$	$0.159^{+0.011}_{-0.008}$
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0 ± 0.2	$0.669^{+0.009}_{-0.008}$
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0 to 15°	0 to 15°

P64C-70-750A,C-3

64 PIN PLASTIC QFP ($\square$14)

detail of lead end

NOTE

1. Controlling dimension —— millimeter.

2. Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	$0.37^{+0.08}_{-0.07}$	$0.015^{+0.003}_{-0.004}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.17^{+0.08}_{-0.07}$	$0.007^{+0.003}_{-0.004}$
N	0.10	0.004
P	2.55±0.1	0.100±0.004
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	2.85 MAX.	0.113 MAX.

P64GC-80-AB8-4

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★ **APPENDIX A. DEVELOPMENT TOOLS**

The following development tools are available for system development using the μPD780988 Subseries.
Also refer to **(5) Cautions on Using Development Tools**.

(1) Language Processing Software

RA78K/0	Assembler package common to 78K/0 Series
CC78K/0	C compiler package common to 78K/0 Series
DF780988	Device file for μPD780988 Subseries
CC78K/0-L	C compiler library source file common to 78K/0 Series

(2) Flash Memory Writing Tools

Flashpro II (part No. FL-PR2), Flashpro III (part No. FL-PR3, PG-FP3)	Flash programmer dedicated to on-chip flash memory microcontroller
FA-64CW FA-64GC	Adapter for flash memory writing

(3) Debugging Tools
• When IE-78K0-NS in-circuit emulator is used

IE-78K0-NS	In-circuit emulator common to 78K/0 Series
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS
IE-78K0-NS-PA**Note**	Performance board for enhancement and expansion of IE-78K0-NS function
IE-70000-98-IF-C	Interface adapter when PC-9800 series PC (except notebook type) is used as host machine (C bus supported)
IE-70000-CD-IF-A	PC card and interface cable when notebook PC is used as host machine (PCMCIA socket supported)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT™ or compatible as host machine (ISA bus supported)
IE-70000-PCI-IF	Adapter necessary when using PCI bus incorporated personal computer as host machine
IE-780988-NS-EM4	Emulation board to emulate μPD780988 Subseries
IE-78K0-NS-P01	I/O board necessary to emulate μPD780988 Subseries
NP-64CW	Emulation probe for 64-pin plastic shrink DIP (CW type)
NP-64GC NP-64GC-TQ	Emulation probe for 64-pin plastic QFP (GC-AB8 type)
EV-9200GC-64	Conversion socket to connect the NP-64GC and a target system board on which the 64-pin plastic QFP (GC-AB8 type) can be mounted
TGC-064SAP	Conversion adapter to connect the NP-64GC-TQ and a target system board on which the 64-pin plastic QFP (GC-AB8 type) can be mounted
ID78K0-NS	Integrated debugger for IE-78K0-NS
SM78K0	System simulator common to 78K/0 Series
DF780988	Device file for μPD780988 Subseries

Note Under development

- **When IE-78001-R-A in-circuit emulator is used**

IE-78001-R-A	In-circuit emulator common to 78K/0 Series
IE-70000-98-IF-C	Interface adapter when PC-9800 series PC (except notebook type) is used as host machine (C bus supported)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT or compatible as host machine (ISA bus supported)
IE-70000-PCI-IF	Adapter necessary when using PCI bus incorporated personal computer as host machine
IE-78000-R-SV3	Interface adapter and cable when using EWS as host machine
IE-780988-NS-EM4	Emulation board to emulate μPD780988 Subseries
IE-78K0-NS-P01	I/O board necessary to emulate μPD780988 Subseries
IE-78K0-R-EX1	Emulation probe conversion board necessary when using IE-780988-NS-EM4 and IE-78K0-NS-P01 on IE-78001-R-A
EP-78240CW-R	Emulation probe for 64-pin plastic shrink DIP (CW type)
EP-78240GC-R	Emulation probe for 64-pin plastic QFP (GC-AB8 type)
EV-9200GC-64	Socket to be mounted on a target system board made for 64-pin plastic QFP (GC-AB8 type)
ID78K0	Integrated debugger for IE-78001-R-A
SM78K0	System simulator common to 78K/0 Series
DF780988	Device file for μPD780988 Subseries

(4) Real-time OS

RX78K/0	Real-time OS for 78K/0 Series
MX78K0	OS for 78K/0 Series

(5) Cautions on Using Development Tools

- The ID78K0-NS, ID78K0, and SM78K0 are used in combination with the DF780988.
- The CC78K/0 and RX78K/0 are used in combination with the RA78K/0 or DF780988.
- The FL-PR2, FL-PR3, FA-64CW, FA-64GC, NP-64CW, NP-64GC, and NP-64GC-TQ are products made by NAITO DENSEI MACHIDA MFG. CO., LTD. (TEL +81-44-822-3813). Contact an NEC distributor regarding the purchase of these products.
- The TGC-064SAP is a product made by TOKYO ELETECH CORPORATION.
  For further information, contact: Daimaru Kogyo, Ltd.
  Tokyo Electronics Department (TEL +81-3-3820-7112)
  Osaka Electronics Department (TEL +81-6-6244-6672)
- For third-party development tools, see the **78K/0 Series Selection Guide (U11126E)**.
- The host machine and OS suitable for each software are as follows.

Host Machine [OS] Software	PC PC-9800 series [Windows™] IBM PC/AT and compatibles [Japanese/English Windows]	EWS HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™] NEWS™ (RISC) [NEWS-OS™]
RA78K/0	√**Note**	√
CC78K/0	√**Note**	√
ID78K0-NS	√	–
ID78K0	√	√
SM78K0	√	–
RX78K/0	√**Note**	√
MX78K0	√**Note**	√

Note DOS-based software

★ **APPENDIX B. RELATED DOCUMENTS**

- **Documents Related to Devices**

Document Name	Document No.	
	English	Japanese
μPD780988 Subseries User's Manual	U13029E	U13029J
μPD780982, 780983, 780984, 780986, 780988 Data Sheet	U12804E	U12804J
μPD78F0988 Data Sheet	This manual	U12805J
μPD780988 Subseries Inverter Control Application Note	U13119E	U13119J
μPD780988 Subseries Special Function Register Table	–	U12806J
78K/0 Series Instructions User's Manual	U12326E	U12326J
78K/0 Series Instruction Table	–	U10903J
78K/0 Series Instruction Set	–	U10904J

- **Documents Related to Development Tools (User's Manuals)**

Document Name		Document No.	
		English	Japanese
RA78K0 Assembler Package	Operation	U11802E	U11802J
	Assembly Language	U11801E	U11801J
	Structured Assembly Language	U11789E	U11789J
RA78K Series Structured Assembler Preprocessor		EEU-1402	U12323J
CC78K0 C Compiler	Operation	U11517E	U11517J
	Language	U11518E	U11518J
CC78K0 C Compiler Application Note	Programming Know-How	U13034E	U13034J
IE-78K0-NS		To be prepared	To be prepared
IE-78001-R-A		To be prepared	To be prepared
IE-780988-NS-EM4		To be prepared	To be prepared
EP-78240		U10332E	EEU-986
SM78K0 System Simulator Windows Based	Reference	U10181E	U10181J
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092E	U10092J
ID78K0-NS Integrated Debugger Windows Based	Reference	U12900E	U12900J
ID78K0 Integrated Debugger EWS Based	Reference	–	U11151J
ID78K0 Integrated Debugger PC Based	Reference	U11539E	U11539J
ID78K0 Integrated Debugger Windows Based	Guide	U11649E	U11649J

Caution   The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

• **Documents Related to Embedded Software (User's Manuals)**

Document Name		Document No.	
		English	Japanese
78K/0 Series Real-Time OS	Fundamental	U11537E	U11537J
	Installation	U11536E	U11536J
78K/0 Series OS MX78K0	Fundamental	U12257E	U12257J

• **Other Related Documents**

Document Name	Document No.	
	English	Japanese
SEMICONDUCTORS SELECTION GUIDE Products & Packages (CD-ROM)	X13769X	
Semiconductor Device Mounting Technology Manual	C10535E	C10535J
Quality Grades on NEC Semiconductor Devices	C11531E	C11531J
NEC Semiconductor Device Reliability/Quality Control System	C10983E	C10983J
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E	C11892J
Guide to Microcomputer-Related Products by Third Party	–	U11416J

Caution   The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: **Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.**

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: **No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V$_{DD}$ or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.**

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: **Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.**

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Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

• Device availability

• Ordering information

• Product release schedule

• Availability of related technical literature

• Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)

• Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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